REMARKS

The Office Action dated February 9, 2005 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Upon entry of this Response, claims 1-22 will be pending in the present application. Claims 1-2, 5-6, 8-11, 13, 15-18, 20, and 22 are independent claims. Claims 2, 3 and 6 have been amended to more particularly point out and distinctly claim the present invention. No new matter is added. Claims 1-22 are respectfully submitted for consideration.

Claims 2-4, 6, 7, 11 and 12 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Office Action asserted that claims 2, 6, and 11 recite the limitation "receiving a data storage enable signal at a first input to the circuit/flip-flop" is unclear, because it is not understood what "enable signal" is claimed.

As stated above, claims 2, 3 and 6 are amended to particularly point out and distinctly claim the subject matter of the invention. Support for the amendments are found at least on Figure 31. Regarding claim 11, it is respectfully submitted that the phrase referred to in the Office Action "receiving a data storage enable signal at a first input to the circuit/flip-flop," is not recited in claim 11. Therefore, it is respectfully submitted that claim 11 particularly points out and distinctly claims the subject matter of

the invention in its current form. Accordingly, withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

Claims 1, 5, 8-10, 13, 14 and 16-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,756,010 to Nelson (Nelson) in view of U.S. Patent No. 4,740,962 to Kish. (Kish). In the Office Action, it was acknowledged that Nelson fails to teach transmitting glitchless fractional clock pulse from the circuit to a data storage element and storing data in the element upon receiving [a] glitchless fractional clock pulse. However, it was alleged in the Office Action Kish may be combined with Nelson to produce the claimed invention. This rejection is respectfully traversed.

Claim 1, recites a method for storing data. The method includes generating a glitchless fractional clock pulse in a circuit, wherein the glitchless fractional clock pulse is of a shorter period than a system core clock pulse, transmitting the glitchless fractional clock pulse from the circuit to a data storage element, and storing data in the storage element upon receiving the glitchless fractional clock pulse.

Claim 5 recites a method for storing data. The method includes generating a glitchless fractional clock pulse in a circuit, transmitting the glitchless fractional clock pulse from the circuit to a data storage element and storing data in the storage element upon receiving the glitchless fractional clock pulse, wherein the data storage element further comprises at least one latch.

Claim 6, upon which claim 7 depends, recites a method for storing data. The method includes generating a glitchless fractional clock pulse in a circuit, transmitting the glitchless fractional clock pulse from the circuit to a data storage element and storing data in the storage element upon receiving the glitchless fractional clock pulse. In the method, the step of generating the glitchless fractional clock pulse further includes receiving a clock signal at a first input to the circuit, the clock signal having a plurality of equally spaced and timed pulses, each of the pulses having a rising edge and a falling edge. The method further includes receiving a data signal at a second input to the circuit and generating the glitchless fractional clock pulse on an output of the circuit in response to the data storage enable signal, wherein a duration of the glitchless fractional clock pulse is less than a duration of the clock signal pulse and is positioned between the rising edge and falling edge of a corresponding clock pulse.

Claim 8 recites a method for storing data. The method includes generating a glitchless fractional clock pulse in a circuit, transmitting the glitchless fractional clock pulse from the circuit to a data storage element and storing data in the storage element upon receiving the glitchless fractional clock pulse, wherein the step of generating a glitchless fractional clock pulse further includes generating a glitchless fractional clock pulse having a period less than a period of a system core clock pulse.

Claim 9 recites a method for storing data. The method includes generating a glitchless fractional clock pulse in a circuit, transmitting the glitchless fractional clock pulse from the circuit to a data storage element and storing data in the storage element

upon receiving the glitchless fractional clock pulse. In the method, generating the glitchless fractional clock pulse further includes generating the glitchless fractional clock pulse, wherein the glitchless fractional clock pulse is generated between a rising edge and a falling edge of a system core clock pulse.

Claim 10 recites a method for enabling a latch. The method includes receiving a clock signal in a logic circuit, receiving a latch enable pulse in the logic circuit, generating a glitchless fractional clock pulse in the logic circuit in response to the latch enable pulse and the clock signal, wherein the glitchless fractional clock pulse is of a shorter period than a system clock core pulse. The method further includes transmitting the glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable time period.

Claim 11, upon which claim 12 depends, recites a method for enabling a latch. The method includes receiving a clock signal in a logic circuit, receiving a latch enable pulse in the logic circuit, generating a glitchless fractional clock pulse in the logic circuit in response to the latch enable pulse and the clock signal and transmitting the glitchless fractional clock pulse to a gate input of a latch to enable the latch to store data during an optimally stable time period. In the method, the step of generating a glitchless fractional clock pulse further includes receiving the latch enable signal at a first input of a first flip flop, receiving the clock signal a second input of a second flip-flop and at a second input of the first flip-flop, receiving an output of the first flip-flop at a first input of the second flip-flop and a first input of an AND gate, receiving an output of the second flip-flop at a

second inverted input of the AND gate and generating the glitchless fractional clock pulse at an output of the AND gate.

Claim 13, upon which claim 14 depends, recites an apparatus for storing data. The apparatus includes at least one storage element having a data input, a storage enable input, and a data output, and at least one logic circuit having an activating input, a clock input, and a logic output. In the apparatus the at least one logic circuit generates a glitchless fractional clock pulse on the logic output, the logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time. In the apparatus, the glitchless fractional clock pulse is of a shorter period than a system core clock pulse.

Claim 16 recites an apparatus for storing data. The apparatus includes at least one storage element having a data input, a storage enable input, and a data output. The apparatus further includes at least one logic circuit having an activating input, an clock input, and a logic output. In the apparatus, the at least one logic circuit generates a glitchless fractional clock pulse on the logic output, the logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time. In the apparatus the glitchless fractional clock pulse generated at the logic output of the AND gate further includes a glitchless fractional clock pulse having a width that is less than a

width of a system clock pulse and positioned between a rising edge and a falling edge of the system clock pulse.

Claim 17, upon which claim 19 depends, recites a network switch for switching data. The network switch includes at least one data port interface, at least one storage element in connection with the at least one data port interface and having a data input, a storage enable input, a data output. In the network switch the at least one logic circuit having an activating input, a clock input, and a logic output. The at least one logic circuit is configured to generate a glitchless fractional clock pulse on the logic output, the logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time. In the network switch, the glitchless fractional clock pulse is of a shorter period than a system core clock pulse.

Claim 18 recites a network switch for switching data. The network switch includes at least one data port interface, at least one storage element in connection with the at least one data port interface and having a data input, a storage enable input, and a data output. In the network switch the at least one logic circuit has an activating input, a clock input, and a logic output. Further, in the network switch the at least one logic circuit is configured to generate a glitchless fractional clock pulse on the logic output, the logic output being connected to the storage enable input of the storage element and operating to enable the at least one storage element to store data resident on the data input at an optimally stable time. The network switch further includes a communication

channel in connection with the at least one data port interface for communicating data in the network switch.

Claim 20, upon which claim 21 depends, recites an apparatus for storing data. The apparatus includes a storage means for storing data, the storage means having an input for receiving data to be stored, a storage enable input for enabling the storage means, and a data output. The apparatus also includes at least one pulse generating means for generating a glitchless fractional clock pulse, the pulse generating means having an activating input, a clock input, and an output in connection with the storage enable input of the storage means. The pulse generating means generates the glitchless fractional clock pulse that is transmitted to the storage means to enable the storage means to store data at an optimally stable time. In the apparatus, the glitchless fractional clock pulse is of a shorter period than a system core clock pulse.

As discussed in the present specification, the claimed invention allows for storage of data during a predictably stable portion of a clock cycle and also minimizes overhead consumption. It is respectfully submitted that Nelson and Kish, taken either individually or in combination, fail to disclose or suggest the elements of any of the presently pending claims and therefore fail to provide the advantages of the claimed invention.

Nelson discloses an asynchronous/synchronous data receiver circuit. The N clock output of clock circuit 122 is connected to the N clock input of bit loop control logic 116 and to the clock input of flip-flop 118 (see col. 4 lines 8-10). Further, the clock circuit 122 is called the "clock source" in column 4 line 12.

Kish discloses a synchronizer for time division multiplexed data. Kish discloses that an output of clock extractor 32 couples to a clock input of an astable multivibrator and to a first input of a two-input logical OR device 34. An output of OR device 34 couples to a write clock input of FIFO memory 36. Further, Kish discloses a clock generator 38 has a first output which couples to a terminal 72, and a second output that couples to a clock input of a counter 40.

As stated above, the Office Action admitted that Nelson fails to disclose the feature of transmitting glitchless fractional clock pulse from the circuit to a data storage element, and alleged that Kish makes up for this deficiency.

However, Nelson fails to disclose or suggest at least "generating a glitchless fractional clock pulse in a circuit...wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse", as recited in claims 1, 5 and 8-10 of the present application and Kish fails to make up for the deficiencies of Nelson. As discussed above the "core clock pulse" disclosed in Nelson is in fact the output of the clock circuit 122 i.e. the "clock source." The recovered clock signal (F in Figure 3) is not the core clock pulse as alleged in the Office Action. The outputs of the actual clock source, or core clock pulse in Nelson, are shown in Figure 3. Thus, Nelson does not disclose or suggest generating a glitchless fractional clock pulse in a circuit, wherein said glitchless fractional clock pulse is of a shorter period than a system core clock pulse, as recited in claims 1, 5 and 10. It is further submitted that Kish fails to make up for these deficiencies.

Regarding claims 13, 17, 18 and 20 it is respectfully submitted that the cited references are deficient at least for the same reasons discussed above regarding claims 1, 5, 8 and 10. Specifically, the cited references fail to disclose or suggest at least the feature of generating a glitchless fractional clock pulse as recited in claims 13, 17, 18 and 20 (underline added). As discussed above, Nelson does not disclose the generation of a glitchless fractional clock pulse since the circuit disclosed in Nelson does not produce a clock pulse that is fractional (smaller) than the clock source 122 outputs as shown in Figure 3 of Nelson

Regarding claims 14, 19, and 21 it is respectfully submitted that since these claims depend from claims 13, 17 and 20 respectively, these claims are allowable at least for the same reasons as claims 13, 17 and 20.

It is respectfully submitted that the cited references fails to disclose or suggest all of the features recited in claims 1, 5, 8-10, 13, 14 and 16-21. Accordingly, withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

Applicant gratefully acknowledges the indication that claims 15 and 22 are allowed.

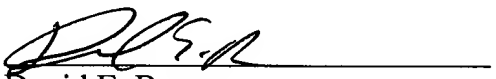
Applicant respectfully submits that all of the issues raised in the Office Action have been addressed and that all of the rejections included in the Office Action have been overcome. Applicant further submits that, at least in view of the above, claims 1-22 of the present application contain allowable subject matter. Therefore, it is respectfully

requested that all claims pending in the present application be allowed and that this application be passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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